
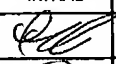

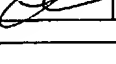
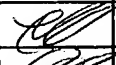


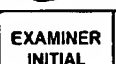


FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. IMEC92.001DV1	APPLICATION NO. 10/766,159
	APPLICANT Brockmeyer, et al.	
	FILING DATE January 27, 2004	GROUP Unknown



U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1.	5,208,673	5/1993	Boyce	—	—	
	2.	5,630,033	5/1997	Purcell et al.	—	—	
	3.	6,028,631	2/2000	Nakaya et al	—	—	

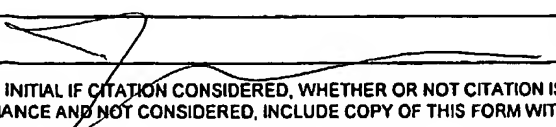
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	4.	EP0698861A1	02/28/95	Europe	—	—		
	5.	EP 0 698 861 A1	02/28/96	Europe	—	—		
	6.	EP0848558A1	07/18/97	Europe	—	—		
	7.	EP 0 848 558 A1	06/17/98	Europe	—	—		

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	8.	Diguett, et al., Formalized methodology for data reuse exploration in hierarchical memory mappings, <i>Proceeding 1997 International Symposium on Low Power Electronics and Design, Monterey, CA USA, Aug. 18-20 1997</i> pp30-35
	9.	Greef, et al., Mapping real-time motion estimation type algorithms to memory efficient, programmable multi-processor architectures, <i>Microprocessing and Microprogramming 41:409-423 (1995)</i>
	10.	Copy of European Search Report; Application No. EP 99 10 4301.
	11.	Greef, et al., Mapping real-time motion estimation type algorithms to memory efficient, programmable multi-processor architectures, <i>Microprocessing and Microprogramming 41 (1995) 409-423.</i>
	12.	IEEE workshop on VLSI signal processing, La Jolla, CA, Oct. 1994. "Global communication and memory optimizing transformations for low power signal processing systems", Cathoor, et al., 12 pages
	13.	IEEE Journal Of Solid-State Circuits, Vol. 31, No. 9, September 1996. "Energy Dissipation in General Purpose Microprocessors" Gonzalez, et al., pages 1277 - 1283
	14.	Proceedings of the IEEE, Vol. 83, No. 2, February 1995. "VLSI Architectures for Video Compression - A Survey". Pirsch, et al., pages 220 - 246
	15.	IEEE Transactions on Circuits and Systems for Video Technology, Vol. 6, No. 1, February 1996. "Architecture and Applications of the HiPAR Video Signal Processor", Ronner, et al., pages 56 - 66
	16.	IEEE Workshop on VLSI signal processing, Monterey, CA, Oct. 1996. "Low Power Storage Exploration for H.263 Video Decoder", Nachtergaele, et al., 12 pages
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	18.	Proc. IEEE Intl. Symp. on Low Power Design, Monterey, Aug. 1996 "Power Exploration for Data Dominated Video Applications", Wuytack, et al., pages 359 - 384
	19.	IEEE Transactions on Circuits and Systems for Video Technology, Vol. 7, No. 1, February 1997. "The M-PEG Video Standard Verification Model", Thomas Sikora, pages 19 - 31

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EXAMINER 	DATE CONSIDERED 9/20/04
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X Did not receive any FOR or NPL.